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Application No.: 10/826,805 Docket No.: JCLA12240

REMARKS

Present Status of the Application

The Office Action rejected claims 1-23. Specifically, the Office Action rejected claims 10

and 21 under 35 U.S.C. 112, second paragraph. The Office Action rejected claims 1, 3-9, 12,

14-20 and 23 under 35 U.S.C. 103(a) as being unpatentable over Murata (U. S. Patent 6,483,184)

in view of Durocher et al. (U. S. Patent 6,614,103, hereinafter Durocher). The Office Action

rejected claims 2, 10-11, 13 and 21-22 under 35 U.S.C. 103 (a) as being unpatentable over

Murata and Durocher and in view of Applicant Admitted prior art (AAPA). Applicants have

amended claims 10 and 21 to overcome the rejections under 35 U.C.C. 112, second paragraph.

Applicants have also added claims 24-25. After entry of the foregoing amendments, claims 1-25

remain pending in the present application, and reconsideration of those claims is respectfully

requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1, 3-9, 12, 14-20 and 23 under 35 U.S.C. 103(a) as being

unpatentable over Murata in view of Durocher. The Office Action rejected claims 2, 10-11, 13

and 21-22 under 35 U.S.C. 103 (a) as being unpatentable over Murata and Durocher and in view

of AAPA. Applicants respectfully traverse the rejections for at least the reasons set forth below.

1. With respect to independent claims 1 and 12, as shown in FIGs. 2-7, for example in FIG.

2B or FIG. 6, the invention is particularly directed to the package of the LED device, which may

include one or several LED chips 210. As one can see, the LED chip has only two electrodes.

Several LED chips can be connected to the same conductive layer 208 at one electrode, so as to

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form an LED array.

The invention uses the conductive layer on sidewall of the grooves 218a, which actually is

a part of the holes 202. Then, the two electrode of the LED chip are coupled to the lower

conductive layer.

As recited in claims 1 and 12, the LED chip represents one LED chip or multiple LED

chips. Each of the LED chip has two electrodes, respectively coupled to the first and the

second patterned conductive films.

2. In re Murata, the package is for a chip with several I/O terminals (Fig. 1 shows four I/O

terminals; FIG. 6 shown several I/O terminals). The elements 20, 26 and 28 are formed for one

conducting lead with respect to the specific I/O terminal. In other words, the elements 20, 26

and 28 are used by the specific L/O terminal but not commonly used by other chips or other L/O

terminals. Murata does not equally disclose the same structure as recited in independent

claims 1 and 12.

3. From the other point of view, Murata is directed to the IC with several I/O leads, and is

not specifically used in LED chip. The specific lead of IC chip in Murata is not commonly

used by other IC chip. Murata actually is nonanalogous to the present invention.

4. In re Durocher, the LED package is disclosed. However, Durocher discloses a different

package structure to the present invention. Also and, Murata is nonanalogous to the LED

package and cannot be directly modified by the disclosure from Durocher. Durocher does not

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specifically provide the motivation of combination with Murata either.

5. With respect to claims 3-9, 14-20 and 23, the features of the number m and n are for

example shown in FIG. 7A. The is particularly the novel design for package of the LED chips.

For at least the same foregoing reasons, Murata is for IC chip and does not disclose the specific

structure used in LED packaging. The Office Action in page 4 only stats that "the prior art

teaches m is a number of the grooves... (emphasis added)" with based on the actual disclosures

by the prior art. However, Applicants have read the disclosures in prior art but cannot find any

this disclosure.

6. Claims 24-25 have defined over the prior art references with at least the foregoing

reasons.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1

and 12 patently define over the prior art references, and should be allowed. For at least the

same reasons, dependent claims 2-11 and 13-25 patently define over the prior art references as

well, wherein claims 3-9, 14-20, and 24-25 further define over the prior art references.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-25 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted, J.C. PATENTS

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